ADCs for Digital Receivers: The Whole World Tunes In

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ABSTRACT

Digital receivers require analog to digital converters with linear transfer functions. Dither is used to remove the effect of encoder non-linearities and increase the effective dynamic range by more than 20 dB on the AD9042. 80 dB dynamic range is shown for analog input frequencies up to 40 MHz, by removing the effects of the input amplifier. Sampling jitter of 300 femto seconds is inferred by observing the increased noise floor level when sampling 201 MHz input signals.

INTRODUCTION

One of the weakest links in a digital receiver has traditionally been the analog to digital converter (ADC). Critical parameters have been size, power dissipation, dynamic range at a given analog input (Ain) frequency, sample rate and cost. The purpose of this paper is to outline recent developments in high dynamic range ADC technology enabling new digital radio developments.

In 1985, the state of the art in commercially available, high dynamic range ADCs was a 12 bit 20 MSPS, 35 sq. inch board. It cost thousands of dollars, dissipated 20W and provided 57 dB dynamic range while digitizing a 5 MHz signal. In 1995, a 12 bit 50 MSPS device can be bought for less than $50 in a plastic package that is smaller than a dime. It can sample a 20 MHz signal at 50 MSPS and provide 80 dB+ dynamic range (See Figure 1.)

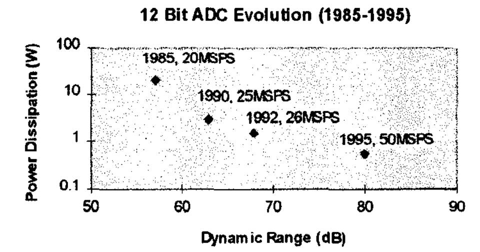

Figure 1: 12 bit ADCs improve with time

The AD9042 is a 12 bit 50 MSPS ADC that dissipates 600 mW from a +5V supply while providing 80 dB of dynamic range (see Figure 2.) It is built on Analog Device's complementary bipolar process (XFCB) with matched 4 GHz NPN, and 2.5 GHz PNP transistors.

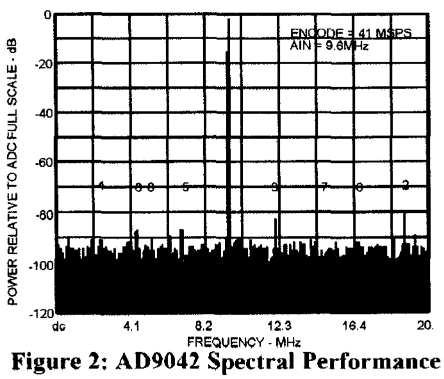

Figure 2: AD9042 Spectral Performance

The simplified block diagram for the ADC is shown in Figure 3. The sources of error in the converter that cumulatively dominate the effective dynamic range, fall into two major groups: 1) Static errors in the ADC encoder, and

2) Dynamic errors originating from the input amplifier (A1) and the first track and hold (TH1). These error sources combine vectorially to define the spurious free dynamic range of the ADC. Static linearity errors in the converter transfer function are not frequency dependent and in the case of the AD9042 are the dominant source of errors at low input frequencies. The dynamic errors predominate at higher analog input frequencies, and increase in magnitude as of the analog input frequency increases.

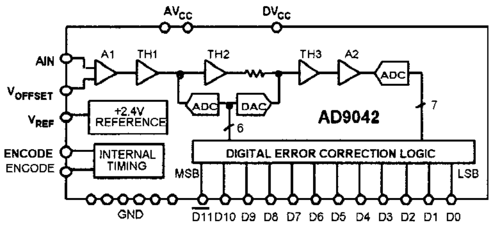

Figure 3: AD9042 Simplified Block Diagram

DITHER

Dither is an uncorrelated signal, usually pseudo random noise, injected into the analog input of the data converter. The use of dither can diminish the effect of static errors on the dynamic range of an ADC. The effect of injecting dither can be to "spread" non-linearities over a wider portion of the ADC transfer function. When transformed into the frequency domain, the effect can be to reduce the spurious level while increasing the noise floor. It is important to understand that the total energy of the static errors are not diminished, they are just moved around. For communications receivers, this can have a profound positive effect.

There are many methods for injecting dither into the ADC system. One method is to introduce the dither so that it occurs out of the band of interest; two obvious locations are at dc and near the Nyquist frequency. One of these locations will typically yield several hundred KHz of bandwidth where noise can be placed.
The purpose of dither is to delocalize or randomize the differential non-linearity (DNL) errors of the converter, such that all of the codes appear more uniform. Figures 5 and 6 show how the DNL is averaged by convolving the PDF of Gaussian dither noise with the DNL transfer function shown in Figure 4. The optimum level of dither for the AD9042 is between 16 and 21.3 codes rms, which correlates to a dither power between -35dBm and -32.5dBm, respectively.

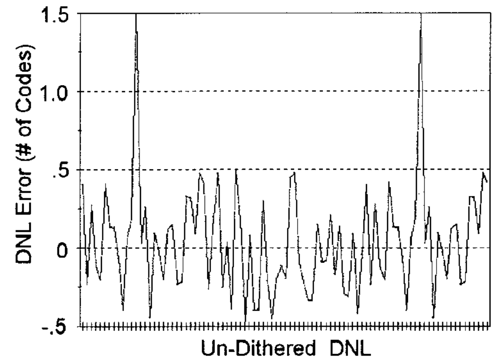

Figure 4: AD9042 DNL, 90 Code span

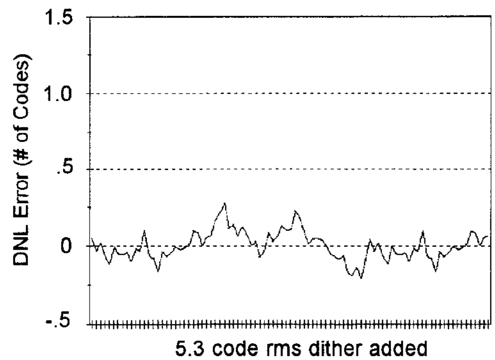

Figure 5: Dithered AD9042 DNL, 90 Code span

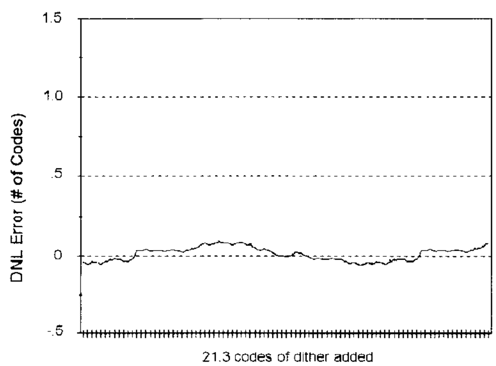

Figure 6: Dithered AD9042 DNL, 90 Code span

DITHER GENERATION

Broadband noise was generated using a noise diode; the power was controlled using a voltage controlled gain amplifier (see Figure 7). The resultant signal was amplified and low pass filtered to locate the dither signal at dc.

Figure 8 shows the spectral performance of an non-dithered AD9042. Figure 9 shows effect of adding dither. Note the magnitude of the dither and the dramatic increase in dynamic range. Dither does not dramatically increase the dynamic range when a full scale Ain signal is processed; it is most effective with small Ain signals found in wide band radio systems Also note that the effective dynamic range greatly exceeds 72 dB, which is sometimes (incorrectly) considered to be the theoretical limit for a 12 bit ADC (12 bits * 6.02 dB/bit.) *This rule of thumb applies to the signal to noise ration (SNR); there is no such limitation for spurious free dynamic range.*

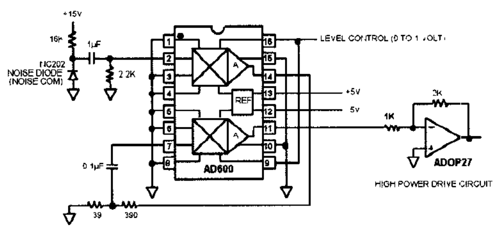

Figure 7: Dither Generation Circuit

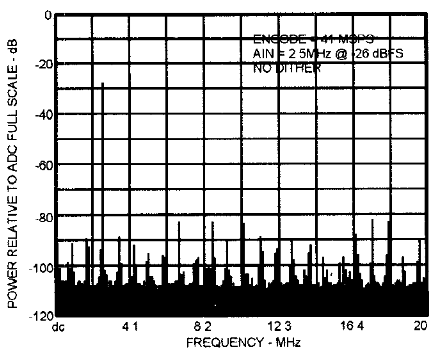

Figure 8: AD9042 FFT; no dither

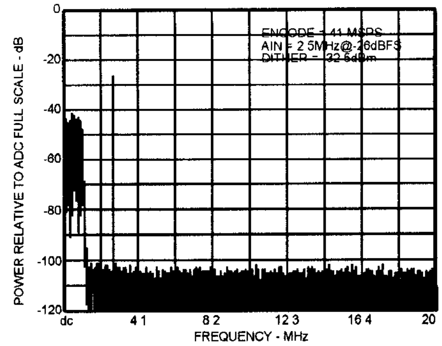

Figure 9: AD9042 FFT; -32.5dBm dither

DYNAMIC LINEARITY

Non-linearities in the encoder transfer function are the major cause of spurs in the AD9042 for low frequency, full-scale Ain signals. At higher Ain frequencies, the input amplifier and track-and-hold are the key sources of harmonic distortion. The input amplifier generates primarily even order harmonics; the odd order harmonics are generated both by the input amplifier and T/H working in tandem. At 20 MHz Ain at full scale, the AD9042 has a dynamic range of 80dB; as the Ain frequency increases, the dynamic range declines. See Figure 10.

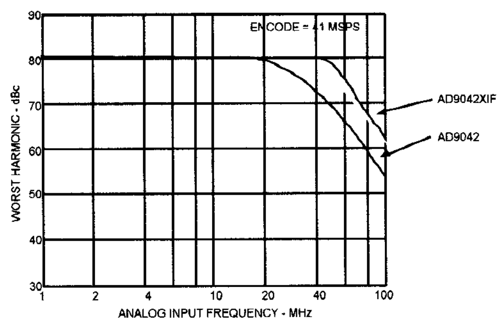

Figure 10: AD9042/AD9042XIF

The AD9042XIF is a close relative of the AD9042; the primary difference is that A1 is left out of the circuit (see Figure 3) allowing direct access to the differential T/H (TH1) This removes the input amplifier as an error source. For Ain frequencies above 20 MHz, the input amplifier diminishes the dynamic range by about 5-8 dB (see figure 10) Figure 11 shows that 78 dB dynamic range has been obtained at 34.5 MHz Ain.

At 200 MHz Ain the worst harmonic is -42 dBc (see Figure 12). The increase in the noise floor seen between the 35 MHz and 201 MHz Ain examples is largely due to the aperture jitter of the on chip T/H, which in the case of the AD9042XIF is about 300 femto seconds With this small amount of sampling error, high IF sampling finally becomes very attractive to systems designers.

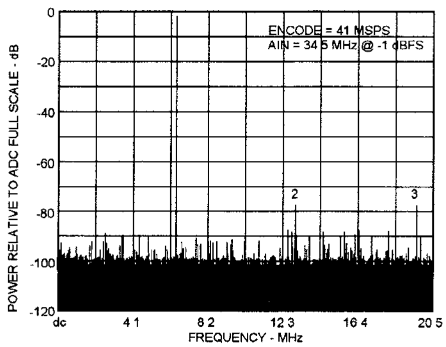

Figure 11: AD9042XIF FFT; 35 MHz Ain

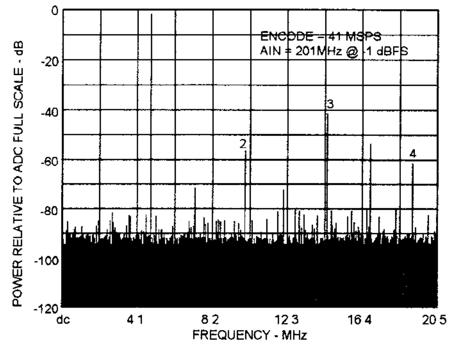

Figure 12: AD9042XIF -sampling 201 MHz

CONCLUSION

The recent advances in sampling technologies, SAW filters, and digital filtering techniques combine to make digital receivers very practical and, most importantly, dramatically less expensive than traditional analog receivers. IF sampling is especially important as it can eliminate mixer down convert stages, and makes the use of SAW filters more practical The high sample rates found in the AD9042 are crucial as they allow more digital processing gain, and in conjunction with IF sampling allow the system designer to move harmonics out of the analysis bandwidth